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| 09/689,532 | 10/12/2000 | Navaz Lulla | 0325.00420 | 9027 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2812 | |

DATE MAILED: 03/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/689,532 | LULLA ET AL. | |
| | Examiner | Art Unit | |
| | Stacy A Whitmore | 2812 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

1. Applicant's arguments filed 12/24/03 have been fully considered but they are not persuasive.

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 3-4, 10, 12, 16-17, 20-22, and 24-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchida (US Patent 5,467,304)

4. As for claim 1, Uchida taught the invention as claimed, including an apparatus comprising:

a logic circuit comprising (i), one or more first inputs each connected to a respective one or more pins, (ii), one or more second inputs each connected to a respective one or more bond options, (iii) one or more third inputs each connected to a respective one or more metal options; and (iv) an output configured to present a plurality of identification codes, wherein said logic circuit is configured to generate a said plurality of identification codes (ID) codes in response to a logical combination of one or more voltage levels on said one or more first inputs, (ii) a state of said one or more bond options, (iii) a state of said one or more metal options [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) –through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5)] and;

a package comprising said one or more pins, wherein said one or more pins are dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs [fig. 1, element 1 – package; fig. 1, elements 9 or 10].

5. As for claim 3, Uchida further taught wherein said circuit is further configured to generate said plurality of ID codes having a number of bits less than a total number of said metal options, bond options, and pins [col. 5, lines 39-43; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33; especially fig. 2, element 8 where ID code is output which is less bits than the metal options, bond options, and pins as cited in the rejection of claim 1].

6. As for claim 4, Uchida further taught wherein said one or more pins are connectable to either a voltage supply power or a voltage supply ground according markings on said package [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33; diffusion of bonding pads of the kinds of circuit corresponds to package markings; especially fig. 2, elements 31, 32, and GRD and VCC of elements 4 and 5].

7. As for claim 10, Uchida further disclosed wherein said apparatus comprises a programmable logic device [fig. 1, element 2, and also 11 for the programmability, as well as the elements 6 and 7 for setting the id of the device].

8. As for claim 12, Uchida further taught wherein said bond options are set based on a style of said package of said apparatus [col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19, and col. 5, lines 23-30, and col. 6, lines 14-33; diffusion of bonding pads of the kinds of circuit corresponds to package markings, kinds correspond to style col. 5, lines 40-41].

9. As for claim 16, Uchida disclosed a method of providing a plurality of ID codes for a single die and package combination [col. 5, lines 23-44; the disclosed portion reads as a single die and package combination because Uchida disclosed One IC chip with multiple kinds or devices] comprising the steps of:

(a) dedicating (i) one or more pins of said package [fig. 1, elements 6, 7 – pins];

(b) generating said plurality of ID codes in response to a logical combination of (i) voltage levels on said one or more pins, (ii) a state of said one or more bond options, and (iii) a state of said one or more metal options [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) –through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5)]; and

c) providing an indication of said voltage levels to be applied to each of said one or more pins [col. 3, lines 62-65].

10. As for claim 17, Uchida disclosed the invention substantially as claimed, including the method of selecting one of a number of ID codes as cited above in the rejection of claim 16.

Uchida further taught wherein step (b) further comprises the steps of:

(b-1) determining said voltage levels on said one or more pins [];

(b-2) determining said state of said one or more metal options [];

(b-3) determining said state of said one or more bond options [].

and logically combining a result of each determining step [].

and (b-4) generating said ID code in response to a logical combination of each determining step [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) –through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5); the voltage levels and options are determined by being input and or being tied to Vcc or GND].

11. As for claim 20, Uchida disclosed an apparatus comprising:

means for generating a plurality of ID codes in response to a logical combination of (i) one or more voltage levels asserted at one or more first inputs, (ii) a state of one or more bond options connected to one or more second inputs and, (iii) a state of one or more metal options connected to one or more third inputs; [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) –through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5)]; and

means for packaging said generating means comprising one or more pins dedicated to providing said one or more voltage levels to respective ones of said one or more first inputs [fig. 1, element 1 – package includes a means for packaging said generating means; [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) –through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5)]].

12. As for claim 21, Uchida disclosed wherein the can present any one of said plurality of ID codes after packaging [abstract; after the assembling process reads as after packaging].

13. As for claim 22, Uchida disclosed wherein said apparatus changes ID code in response to a change in said one or more voltage levels applied to said one or more pins [fig. 3, elements S4-S11, also fig. 2, element 8, which changes according the inputs].

14. As for claim 24, Uchida further disclosed marking voltage level indications on said package after assembly to select a particular one of said plurality of identification codes for said die and package combination [abstract; col. 5, lines 23-30, 40-43; col. 6, lines 8-49; and col. 10, lines 23-33].

15. As for claim 25, Uchida further disclosed changing voltage level indications provided to select different ID codes [abstract; col. 10, lines 23-33].

16. As for claim 26, Uchida discloses wherein: each of said one or more metal options is configured to couple said respective one or said one or more third inputs to one of a pull-up device and a pull-down device [fig. 2, connection of elements 31 and 32 to at least element 10; col. 5, lines 44-48, where the metal options are pull-up devices, therefore coupling to at least element 10, a third input].

17. Claims 2, and 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter referred to as IEEE Std 1149.1).

18. As for claims 2, and 5-9, Uchida disclosed the invention substantially as claimed, including the apparatus, method and means for generating a plurality of ID codes as cited above in the rejections of claims 1, 3-4, 10, 12, 16, 20-22, and 24-25.

As for claims 2, and 5-9, Uchida did not specifically disclose [2] that said ID codes comprise a silicon ID of an electronic part; [5] wherein each of said plurality of ID codes comprises a part number for said apparatus; [6] wherein said part number is combined with other identification codes; [7] wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacturing number; [8] wherein said ID code is captured in a register in response to an identification request; and [9] wherein said register comprises a JTAG ID code register.

IEEE Std 1149.1 disclosed [2] said ID codes comprise a silicon ID of an electronic part [pg. 108, fig. 11-1; pg. 111, section 11.3.1]; [5] wherein each of said plurality of ID codes comprises a part number for said apparatus [pg. 108, fig. 11-1; pg. 111, section 11.3.1]; [6] wherein said part number is combined with other identification codes [pg. 108, fig. 11-1]; [7] wherein said other ID codes comprise one or more codes selected from the group consisting of a version number and a manufacturing number [pg. 108, fig. 11-1]; [8] further comprising a register configured to capture said ID codes from said output of said logic circuit in response to an identification request [pg. 56, section 7.12.1, element c]; and [9] wherein said register comprises a JTAG ID code register [pg. 56, section 7.12.1, element c; and pg. iii, JTAG].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and IEEE Std 1149.1 because both Uchida and IEEE Std 1149.1 both disclose the use of ID codes for the purpose of identifying either different kinds or devices with the use of an ID code register and Uchida further discloses the IEEE Std 1149.1 [Uchida, col. 10, lines 34-41]. Therefore, adding the IEEE Std 1149.1's silicon ID of an electronic part would have ensure that no two components offered in the same package have the same code which would reduce the risk of inserting incorrect parts in locations [see IEEE Standard 1149.1, pg. 11, sections 11.3.1 and 11.3.2]. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and IEEE Std. 1149.1 because utilizing the ID codes in combination with the claimed elements of 2, and 5-9 would have allowed Uchida's system to use the existing abilities of the already existing IEEE Std 1149.1 for functions that are utilized for the programming and testing of IEEE Std.-compliant devices.

19. Claims 11, and 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of Carmichael et al. (US Patent 6,308,311).

20. As for claim 11, Uchida disclosed the invention substantially as claimed, including the apparatus as cited in the rejection of claims 1 and 3, and further disclosed wherein said metal options are not to indicate an operating voltage of said apparatus [abstract; col. 3, lines 14-19; col.'s 5-6, bonding options, also fig. 2, elements 31, 32, and GRD and Vcc of elements 4 and 5].

Uchida did not specifically teach wherein said metal options are set to indicate an operating voltage of said apparatus.

Carmichael taught wherein device ID options are set to indicate an operating voltage of said apparatus [col. 12, line 67 – col. 13, line 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and Carmichael because setting Uchida's metal options with an operating voltage of said apparatus would have improved Uchida's identifying devices for proper operating characteristics and avoid potential damages to devices [see Carmichael, col. 13, lines 15-18].

21. As for claims 13 and 14, Uchida taught the invention substantially as claimed, including the apparatus as cited in the rejection of claim 1.

Uchida did not specifically teach wherein said one or more pins are labeled as either a first or second supply voltage/based on characteristics of said apparatus.

Carmichael taught wherein pins are labeled either a first or second supply voltage based on characteristics of an apparatus [col. 12, line 66 – col. 13, line 4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made

to combine the teachings of Uchida and Carmichael because adding a pin labeled as a first or second supply voltage to Uchida's system would have improved Uchida's system by allowing Uchida's system to adjust operating characteristics (e.g. supply voltage) of different devices, and thereby prevent possible damages due to incorrect supply voltages [see Carmichael, col. 12, lines 45-48].

22. Claims 15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of Carmichael et al. (US Patent 6,308, 311), and further in view of Wegner et al. (US Patent 6,311,246).

23. As for claim 15, Uchida and Carmichael taught the invention substantially as claimed, including the apparatus as cited in the rejections of claims 1, and 13-14 and further disclosed the characteristics of operating voltage and at least one voltage supply pin and at least one ground pins cited in the rejection of claim 14.

Carmichael disclosed a test access port [col. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida and Carmichael because adding Carmichaels test access port would have improved Uchida's system by providing a proven test standard such as Carmichael's IEEE Standard 1149.1 for the control of programmable logic devices [see Carmichael, col. 1, lines 14-20].

Uchida in view of Carmichael did not specifically teach wherein said characteristics comprise one or more characteristics selected from the group consisting of volatility, price, package metal options, internal structure, part category, and density or a test access port.

Wegner taught the cost characteristic and a test access port [col. 1, lines 14-28].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida, Carmichael, and Wegner because adding Wegner's cost characteristic to Uchida in view of Carmichael's system would improve Uchida in view of Carmichael's additional device ID information for the purpose of identifying features of the of similar devices [see Wegner, col. 1, lines 14-20].

24. Claim 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (US Patent 5,467,304) in view of IBM TDB Publication, "Using a portion of the boundary register as the identification register" (hereinafter referred to as IBM), and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990 (hereinafter referred to as IEEE Std. 1149.1).

25. As for claim 18, Uchida in view of IBM disclosed the invention substantially as claimed, including the method of generating ID codes as cited in the rejections of claims 16-17.

Uchida in view of IBM did not specifically disclose c) presenting said ID code in response to an identification request and wherein said ID request comprises a JTAG ID code instruction.

IEEE Std 1149.1 disclosed c) presenting said ID code in response to an identification request and wherein said ID request comprises a JTAG ID code instruction [pg. 55-56, IDCODE and USERCODE instructions which are the requests].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Uchida in view of IBM, and IEEE Std 1149.1 because utilizing the JTAG ID code request in order to present the ID code would have allow Uchida in view of IBM's system to fully use the already existing functionality of the

IEEE 1149.1 standard for the purposes of testing and identifying kinds of devices as disclosed by Uchida.

26. Applicant's arguments filed 12/24/03 with regard to claims 1-26 have been fully considered but they are not persuasive.

In the remarks section applicant argues in substance:

A: Uchida does not disclose a circuit configured to generate a plurality of identification codes (ID) codes in response to a logical combination of (i), one or more first inputs each connected to a respective one or more pins, (ii), a state of one or more second inputs each connected to a respective one of one or more bond options and, (iii) one or more third inputs each connected to a respective one or more metal options; and an output configured to present a plurality of identification codes.

The examiner respectfully disagrees for the following reasons:

As to point A: Uchida discloses a circuit configured to generate a plurality of identification codes (ID) codes in response to a logical combination of (i), one or more first inputs each connected to a respective one or more pins, (ii), a state of one or more second inputs each connected to a respective one of one or more bond options and, (iii) one or more third inputs each connected to a respective one or more metal options; and an output configured to present a plurality of identification codes [fig. 1, elements 3,4, and 5 – make up the circuit; col. 3, line 66 – col. 4, line 5; also, col. 3, lines 6-19; col. 5, lines 23-30; and col. 6, lines 14-33; also from fig. 2, the logical combination of (i) – through (iii) is comprised of the combination of elements 6-7 (bonding options), one or more voltage levels (elements 9 or 10); and a state of one or more metal options (elements 31, 32, or GRD in element 4 or Vcc in element 5); See also as cited in the rejection of claim 1 and applicants remarks on page 9 of the amendment dated 12/24/03.

27. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stacy A Whitmore
Primary Examiner
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